#17E Abruption 3/18/2002

S/N 09/551,027 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner:	Michael Trinh
Serial No.:	09/551,027	Group Art Unit:	2822
Filed:	April 17, 2000	Docket:	303.379US2
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on November 21, 2001. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendments of previously pending claims 20, 25, 41, 49, 51, 53, and 55. The specific amendments to individual claims are detailed in the following marked up set of claims.

20. (Three Times Amended) A method of fabricating a memory array, the method comprising the steps of:

forming from a single unbonded substrate a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein each access transistor includes, in order, a first source/drain region, a body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor in a trench without forming an implanted barrier region in the substrate, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor;

forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line